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**ABSTRACT OF THE DISCLOSURE**

**TYPE CONFIGURABLE MEMORY METHODOLOGY FOR USE WITH METAL  
PROGRAMMABLE DEVICES**

5

A pre-diffused array of core memory cells is provided in a metal programmable device. Multiple control block versions of interface logic are also provided and placed around the memory core. Contact points for each control block are brought to the surface of the wafer using a via. The appropriate interface logic is selected by connecting the metal layer to the appropriate surface

10 contacts to access the core memory cells. The application-specific circuit, including memory configuration and memory interface type, is programmed with the metal layer.